VLSI Design Final Syllabus

SEQUENTIAL CIRCUITS:

Design with transmission gate, function and timing diagram:

i) CMOS positive-level-sensitive D Latch
ii) CMOS negative-level-sensitive D Latch
iii) CMOS positive-edge-triggered D Flip-Flop
iv) CMOS negative- edge-triggered D Flip-Flop

Define the terms corresponding to VLSI Design: Regularity, Modularity, and Locality

PHYSICAL DESIGN AUTOMATION:

Objective; New Trends in VLSI Design Cycle; Physical Design Cycle (Flow diagram and definition of different steps)

DESIGN STYLES (Description in short and difference among them):

i) Full-Custom
ii) Standard Cell
iii) Gate Arrays
iv) Field Programmable Gate Arrays

FLOORPLANNING MODEL:

Slicing floorplans and non-slicing floorplans (Definition, Classification and example)

Polish expression, normalized Polish expression (Definition with example)

Neighborhood structure: three types of operations to perturb one normalized Polish expression to another (Mention the types with example).

Cost function (Solve the problems)

PARTITIONING:

Three broad parameters for efficiency of partitioning;

Net and Netlist (Definition)

LEVEL OF PARTITIONING: Description of different levels

Disadvantages of the bad partitioning process

Two Well-known local methods for partitioning are:

- Kernighan-Lin algorithm (K-L algorithm)and
- Fiduccia-Mattheyses algorithm (F-M algorithm)

Drawbacks of K-L algorithm and Features of F-M algorithm.

ROUTING:

Objectives of routing problem;

Steiner Tree and Rectilinear Steiner Tree (Definition and example)

Classification of Routing. Features of Global and Detailed Routing.

Description of Pin Assignment and Region Assignment in Global Routing with example.

STICK DIAGRAMS:

Definition

Draw Stick diagram of a CMOS Inverter and 2 input NAND gate.

Rules of drawing Stick diagrams

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